

**PATENT**

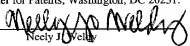
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re application of: ) Docket No: LAM1P106D  
)  
Uglow, et al. )  
)  
Application No: Unknown ) Group Art Unit: Unknown  
)  
Filed: February 16, 2001 ) Examiner: Unknown  
)  
15 For: METHODS FOR MAKING DUAL- )  
DAMASCENE DIELECTRIC )  
STRUCTURES (as amended) )  
Date: February 16, 2001  
\_\_\_\_\_ )

**CERTIFICATE OF EXPRESS MAILING**

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on February 16, 2001 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR § 1.10, Mailing Label Number EL610160873US, addressed to: Commissioner for Patents, Washington, DC 20231.

Signed:   
Neely J. Wells

**PRELIMINARY AMENDMENT**

Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

The following is a preliminary amendment. Please enter the following amendments and remarks:

**IN THE TITLE**

Please amend the title to: --DUAL-DAMASCENE DIELECTRIC  
STRUCTURES--.

**IN THE SPECIFICATION**

Please amend the specification as follows:

Page 10, line 10, please delete “etch” and insert --etched--.

5 Page 11, line 17, please insert --(see Figure 3)-- after “108a”.

Page 12, line 13, please insert --(see Figure 4)-- after “108b”.

Page 12, line 16, please insert -- as shown in Figure 4,-- after “104”.

Page 13, line 3, please delete “exposed” and insert --expose--.

Page 13, line 11, please insert --as shown in Figure 5-- after “photoresist”.

10 Page 13, line 11, please delete “As shown in Figure 10,” and insert --Figure 10A  
illustrates subsequent fabrication in which--.

Page 15, line 12, please delete “etch” and insert --etched--.

**IN THE CLAIMS**

15 All claims pending after this amendment are listed below. Please amend the  
claims as follows:

**PLEASE CANCEL CLAIMS 1-20.**

20 21. (Amended) A multi-layer dielectric layer over a substrate for use in dual-  
damascene applications, comprising:

a barrier layer disposed over the substrate;

an inorganic dielectric layer disposed over the barrier layer; and

25 a low dielectric constant layer disposed directly over the inorganic dielectric layer;

wherein the [inorganic] low dielectric constant layer is configured to receive  
metallization line trenches and the [low] inorganic dielectric [constant] layer is  
configured to receive vias during a dual-damascene process.

22. A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 21, wherein the barrier layer is one of a silicon nitride layer and a silicon carbide layer.

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23. A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 22, wherein the inorganic dielectric layer is one of an undoped TEOS oxide and a fluorine doped oxide.

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24. A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 23, wherein the low dielectric constant layer is a carbon doped oxide.

**PLEASE CANCEL CLAIM 25.**

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26. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 24, wherein the inorganic dielectric layer has different material properties than the low dielectric constant layer.

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27. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 26, wherein a thickness of the inorganic dielectric layer is about 4500 Angstroms.

28. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 27, wherein a thickness of the low dielectric constant layer is about 5000 Angstroms.

29. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 26, wherein a thickness of the low dielectric constant layer is greater than a thickness of the inorganic dielectric layer.

30. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications as recited in claim 29, wherein the thickness of the inorganic dielectric layer is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer and the inorganic dielectric layer is about 10,000 Angstroms.

31. (New) A multi-layer inter-metal dielectric semiconductor structure, comprising:

a barrier layer disposed over a base dielectric layer;

an inorganic dielectric layer of an un-doped TEOS oxide disposed over the barrier layer;

a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer;

wherein the low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

32. (New) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 31, wherein a thickness of the inorganic dielectric layer of an un-doped TEOS oxide is about 4500 Angstroms.

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33. (New) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 32, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is about 5000 Angstroms.

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34. (New) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 31, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of an un-doped TEOS oxide.

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35. (New) A multi-layer inter-metal dielectric semiconductor structure as recited in claim 34, wherein the thickness of the inorganic dielectric layer of an un-doped TEOS oxide is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer of a carbon doped oxide and the inorganic dielectric layer of an un-doped TEOS oxide is about 10,000 Angstroms.

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36. (New) A dielectric structure for dual-damascene applications, comprising:  
a barrier disposed over a base dielectric;  
an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier;

a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer;

wherein the low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

37. (New) A dielectric structure for dual-damascene applications as recited in claim 36, wherein a thickness of the inorganic dielectric layer of a fluorine doped oxide is about 4500 Angstroms.

38. (New) A dielectric structure for dual-damascene applications as recited in claim 37, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is about 5000 Angstroms.

39. (New) A dielectric structure for dual-damascene applications as recited in claim 36, wherein a thickness of the low dielectric constant layer of a carbon doped oxide is greater than a thickness of the inorganic dielectric layer of a fluorine doped oxide.

40. (New) A dielectric structure for dual-damascene applications as recited in claim 39, wherein the thickness of the inorganic dielectric layer of a fluorine doped oxide is about at least 1,000 Angstroms, and the thickness of the low dielectric constant layer of a carbon doped oxide and the inorganic dielectric layer of a fluorine doped oxide is about 10,000 Angstroms.

41. (New) A multi-layer dielectric layer over a substrate for use in dual-damascene applications, comprising:

a barrier layer disposed over the substrate;

an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier

5 layer; and

a low dielectric constant layer of a carbon doped oxide disposed directly over the inorganic dielectric layer;

wherein a thickness of the inorganic dielectric layer of a fluorine doped oxide is about 4500 Angstroms and is configured to receive vias, and wherein a thickness of the  
10 low dielectric constant layer of a carbon doped oxide is greater than the thickness of the inorganic dielectric layer of a fluorine doped oxide and is configured to receive metallization line trenches during a dual-damascene process.

15 **REMARKS**

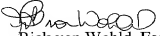
Claims 21-24, and 26-41 are pending after entry of this preliminary amendment. Claims 1-20 and 25 have been cancelled. New claims 26-41 have been added, and no new matter is presented.

20 The Specification is herein amended to correct typographical errors and minor omissions in order to more clearly and accurately describe the claimed invention. No new matter has been introduced.

This preliminary amendment is filed with a divisional application of Application Number 09/346,156, filed on June 30, 1999. This divisional application is being filed  
25 under 37 C.F.R. §1.53(b).

Applicants respectfully submit that all of the pending claims are in a condition for allowance, and a notice of allowance is respectfully requested. If the Examiner has any questions concerning the present preliminary amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with this filing, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106D). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,  
MARTINE PENILLA & KIM, LLP

  
Rick von Wohld, Esq.  
Reg. No. P-48,018

710 Lakeway Drive, Suite 170  
Sunnyvale, CA 94085  
Telephone: (408) 749-6900  
Facsimile: (408) 749-6901  
**Customer No. 25920**